REMARKS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 1-3 and 5 remain pending in the application. Claims 1-3 and 5 are amended, and Claims 4 and 6 are canceled without prejudice or disclaimer by the present amendment. No new matter is presented.[1]

In the Office Action, Claims 1-2 were rejected under 35 U.S.C. § 102(b) as anticipated by Kutaragi et al. (U.S. Patent No. 5,111,530, hereinafter "Kutaragi"); and Claims 3-6 were rejected under 35 U.S.C. § 103(a) as unpatentable over Kutaragi in view of Davis et al. (U.S. Patent No. 4,991,169, hereinafter "Davis").

In light of the several grounds of rejection on the merits, independent Claims 1-3 and 5 have been amended to clarify the claimed invention and to thereby more clearly patentably define over the applied references.

Amended Claim 1 recites a data processor including, in part, a CPU, a DSP, and an external memory, in which

> when the DSP accesses the external memory using a maximum number of the bus cycles in a unit of data access wherein the DSP actually accesses the external memory, access from the CPU to the external memory is placed in a wait state until a subsequent unit of data access commences, and
>
> when the DSP does not access the external memory using the maximum number of the bus cycles in said unit of data access wherein the DSP actually accesses the external memory, access from the CPU to the external memory is constantly allowed during said unit of data access.

Applicant respectfully submits that Kutaragi fails to disclose or suggest these features.

Kutaragi concerns an apparatus in which "displacement of the access periods can be properly adjusted by the switching control of the switches 97 to 99 by the time-division

[1] The amendment to Claim 3 finds support at least in Claim 4. The amendment to Claim 5 finds support at least in Claim 6.

control circuit 94 and the latch operations of the latch circuits 10a and 13a."[2] Further, the Kutaragi

> time-division control circuit 94 generates such a switching control signal . . . that on the basis of the time-division signal . . . , the movable contacts 97m, 98m and 99m of the switches 97, 98 and 99 are connected to the first fixed contacts 97a, 98a and 99a during the first access period M_{D1}' and the second access period M_{D2}' of the external RAM 14 and that the movable contacts 97m,98m and 99m of the switches 97, 98 and 99 are connected to the second fixed contacts 97b, 98b and 99b during the third access period M_C'.[3]

Kutaragi merely describes adjusting the access periods such that the movable contacts are connected to the first fixed contacts during the first and second access periods and that the movable contacts are connected to the second fixed contacts during the third access period. Applicant submits that Kutaragi fails to disclose that "when the DSP does not access the external memory using the maximum number of the bus cycles in said unit of data access wherein the DSP actually accesses the external memory, access from the CPU to the external memory is constantly allowed during said unit of data access," as recited in amended Claim 1.

Indeed, the Office appears to acknowledge that Kutaragi fails to disclose the external memory access recited in Claim 1. Rather, the Office asserts that "the [Kutaragi] time-division control circuit ***can*** adjust the memory bus to be accessed the DSP only . . . ."[4] The Office also asserts that "Kutaragi clearly states that the amount of cycles usable by the DSP . . . ***can*** be adjusted such that the DSP accesses the memory during the entire access period."[5]

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[2] Kutaragi, col. 16, ll. 31-34.
[3] Id, ll. 35-45.
[4] Office Action at 4, ll. 11-13 (emphasis supplied).
[5] Advisory Action at 2, ll. 4-5 (emphasis supplied).

Applicant submits that Kutaragi merely teaches connecting the movable contacts to the first fixed contacts during the first and second access periods and to the second fixed contacts during the third access period. Applicant additionally submits that Kutaragi fails to suggest the modifications proposed by the Office. Accordingly, it appears that the Office has engaged in improper hindsight reasoning by relying on knowledge gleaned only from Applicant's specification.[6] It is therefore submitted that the Office has failed to establish a *prima facie* case of obviousness in rejecting the features of Claim 1.

Applicant respectfully submits that Kutaragi fails to suggest that "when the DSP does not access the external memory using the maximum number of the bus cycles in said unit of data access wherein the DSP actually accesses the external memory, access from the CPU to the external memory is constantly allowed during said unit of data access," as recited in amended Claim 1.

Therefore, it is respectfully submitted that amended Claim 1 patentably distinguishes over Kutaragi. Applicant further submits that amended Claim 2 patentably defines over Kutaragi for at least the same reasons as discussed with regard to Claim 1 and for the more detailed features presented by Claim 2.

Claim 3 is amended to include elements previously recited in Claim 4. Amended Claim 3 recites a data processor including, in part,

> an access determination unit configured so that when each of the DSPs issues the read command or the write command at the same time, none of the DSPs are not allowed to access the external memory and when the only one of the DSPs issues the read command or the write command, the only one DSP is allowed to access the external memory . . . .

Applicant respectfully submits that Kutaragi and Davis fail to disclose or suggest these features.

[6] In re McLaughlin 443 F.2d 1392, 1395 (CCPA 1971); MPEP 2145 X. A.

The Office concedes that "Kutaragi does not teach multiple DSPs with a shared RAM."[7] Applicant respectfully submits that Kutaragi fails to disclose or suggest a read/write control unit and an access determination unit as recited in amended Claim 3.

Davis concerns "time staggered cyclic timing signals A, B, C, and D,"[8] with which "Address multiplexor 114 is operated by signals C+D to initiate data accesses for processor 21 during A and B times and processor 20 during C and D times."[9]

That is, the multiplexer of Davis initiates data accesses for processor 21 and processor 20 during mutually exclusive times.[10] There is no teaching nor suggestion in Davis of the access to the external memory recited in amended Claim 3.

Rather, the Office asserts that "'Configured to' is not a positive recitation, and as long as the access determination unit is able to perform a function it is construed as 'configured to' to perform a function."[11] Applicant respectfully traverses this assertion, because a claim directed to a system or structure may define the configuration of its elements rather than a present action that the system or structure is performing. For example, the binding decision by the United States Court of Customs and Patent Appeals held that the use of the words "adapted to" indicate a structural element. The Court explained,

> The claimed invention does include present structural limitations on each part . . . . For example, paragraph two of claim 31 calls for "a pair of sleeves . . . each sleeve of said pair *adapted to be fitted* over the insulating jacket of one of said cables." Rather than being a mere direction of activities to take place in the future, this language imparts a structural limitation to the sleeve. Each sleeve is so structured or dimensioned that it can be fitted over the insulating jacket of a cable. A similar situation exists with respect to the "adapted to be affixed" and "adapted to be positioned" limitations in the third and fourth paragraphs of the claim.[12]

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[7] Office Action at 8, l. 1.
[8] Davis, col. 9, ll. 31-32.
[9] Id., ll. 51-54.
[10] See also id., Fig. 2.
[11] Advisory Action at 2, ll. 9-10.
[12] In re Venezia, 189 USPQ 149, 151-52 (CCPA 1976).

Thus, Applicant submits that the use of the phrase "configured to"--like "adapted to"--in Claims 3 and 5 imparts a structural feature because it describes the system's present structural configuration rather than a mere direction of activities to take place in the future.

Additionally, it is well established that each word of every claim must be given weight.[13]

Thus, it would be without merit to suggest that the "configured to" language is not a positive recitation of the structures recited in Claims 3 and 5.

Thus, it is respectfully submitted that Davis fails to teach or suggest "an access determination unit configured so that when each of the DSPs issues the read command or the write command at the same time, none of the DSPs are not allowed to access the external memory and when the only one of the DSPs issues the read command or the write command, the only one DSP is allowed to access the external memory," as recited in amended Claim 3.

Therefore, Kutaragi and Davis fail to disclose or suggest "an access determination unit," as recited in amended Claim 3. Applicant respectfully submits that amended Claim 3 patentably distinguishes over Kutaragi and Davis.

It is further submitted that amended Claim 5 patentably defines over Kutaragi and Davis for the same reasons as discussed above with regard to Claim 3 and for the more detailed features presented by Claim 5.

[13] See In re Wilson, 424 F.2d 1382, 1385 (CCPA 1970).

Consequently, in view of the present amendment and in light of the foregoing comments, it is respectfully submitted that the invention defined by Claims 1-3 and 5 patentably distinguishes over the applied references. The present application is therefore believed to be in condition for formal allowance. An early and favorable reconsideration of the application is respectfully requested.

Respectfully submitted,

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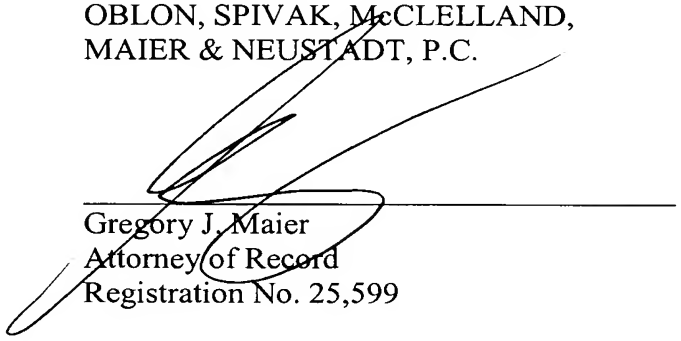

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